AMENDMENTS TO THE SPECIFICATION

Please replace the title of the invention with the following title written in amendment format:

DATA PROCESSING SYSTEM WITH ~~PARTIAL~~ BYPASS REORDER BUFFER HAVING NON-BYPASSABLE LOCATIONS AND COMBINED LOAD/STORE ARITHMETIC LOGIC UNIT AND PROCESSING METHOD THEREOF

Please amend paragraph [0009] as follows:

[0009] According to one aspect of the invention, a data processing system for executing a plurality of instructions having a prescribed program order comprises a register file, a reorder buffer, and a plurality of functional units. The register file includes a plurality of registers to store data. The reorder buffer includes N buffer locations of which M buffer locations are bypassable and N-M buffer locations are non-bypassable, wherein N and M are integers and N > M. Each functional unit is capable of executing instructions regardless of the prescribed program order. The reorder buffer temporarily stores data corresponding to the plurality of instructions. When data of one of the plurality of instructions to be executed by a corresponding one of the plurality of ~~functions units~~ functional units is temporarily stored in one of the M bypassable buffer locations, the reorder buffer transfers the in one of the bypassable M buffer locations to the corresponding one of the functional units in order to execute the instruction. The register file also stores data corresponding to retired ones of the plurality of instructions.